

SUB C.7  
a first copper layer directly on the first titanium layer;  
a titanium passivation layer directly on the first copper layer at  
non-solder bump locations; and  
under bump material directly on the first copper layer at solder  
bump locations.

7. (New) A wafer in accordance with claim 6 further comprising solder  
bumps on the under bump material.

B1  
8. (New) A chip device comprising:  
a non-passivated die;  
a first titanium layer at non-isolation locations on the die;  
a first copper layer directly on the first titanium layer;  
a titanium passivation layer directly on the first copper layer at  
non-solder bump locations; and  
under bump material directly on the first copper layer at solder  
bump locations.

9. (New) A chip device in accordance with claim 8 further comprising  
solder bumps on the under bump material.

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REMARKS

Claims 6-9 are pending.

Claims 1 and 3 stood rejected under 35 U.S.C. § 102(b) as being  
anticipated by Mizuhara et al. (U.S. Patent No. 5,898,221).

Claims 1 and 3 stood rejected under 35 U.S.C. § 102(e) as being  
anticipated by Wang et al. (U.S. Patent No. 6,362,087).

Claim 2 stood rejected under 35 U.S.C. § 103(a) as being unpatentable  
over Mizuhara et al.